In the Claims:

1. (Currently Amended) In a method of making a dual work function gate electrode of a CMOS semiconductor structure, the improvement comprising formation of the dual work function gate electrode so that there is no boron penetration in the channel region and no boron depletion near the gate oxide, comprising:

a) forming a gate oxide layer over a channel of a nMOS site and over a channel of a pMOS site;

b) forming an undoped polysilicon layer over said gate oxide layer;

c) masking said pMOS site, forming an a-Si layer over said nMOS site by implanting a first heavy ion into selected from the group consisting of Ge and Si, a top portion of said undoped polysilicon to form said a-Si layer over a remaining layer of undoped polysilicon between said gate oxide layer and said a-Si layer, and implanting arsenic solely into said a- Si layer;

d) masking said nMOS site formed by step c), forming an a-Si layer over said pMOS site by implanting a second heavy ion selected from the group consisting of Ge and Si, into a top portion of said undoped polysilicon to form said a-Si layer over a remaining layer of undoped polysilicon between said gate oxide layer and said a-Si layer, and implanting boron solely into said a –Si regions;

e) laser annealing said nMOS and pMOS sites for a ~~sufficient~~ period of time between about 40ns and 80ns, and at an energy level sufficient to melt at least a portion of the a-Si but insufficient to melt the polysilicon; and

f) affecting cooling after laser annealing to convert a- Si into polysilicon without gate oxide damage.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Previously Presented) The method of claim 11 wherein said laser energy level sufficient to melt at least a portion of a- Si but insufficient to melt said polysilicon is between about 0.3 J/cm^2 to about 0.7 J/cm^2.

6. (Original) The method of claim 5 wherein in step d) said boron implanting in said a- Si regions is in a concentration range from about 1×10^{19} cm^{-3} to about 5×10^{20} cm^{-3}.

7. (Currently Amended) The method of claim 1 ~~claim 2~~ wherein said first heavy ion implantation is affected by using Ge.

8. (Currently Amended) The method of claim 1 ~~claim 2~~ wherein said first heavy ion implantation is affected using Si.

9. (Currently Amended) The method of claim 1 ~~claim 3~~ wherein said second heavy ion implantation is affected using Ge.

10. (Currently Amended) The method of claim 1 ~~claim 3~~ wherein said second heavy ion implantation is affected using Si.

11. (Previously Presented) In a method of making a dual work function gate electrode of a CMOS semiconductor structure, the improvement comprising formation of the dual work function gate electrode so that there is no boron penetration in the channel region and no boron depletion near the gate oxide, comprising:

a) forming a gate oxide layer over a channel of a nMOS site and over a channel of a pMOS site;

b) forming an undoped polysilicon layer over said gate oxide layer;

c) masking said pMOS site, forming an a-Si layer over said nMOS site using a first heavy ion implantation with a material selected from the group consisting of Ge and Si, and implanting arsenic solely into said a- Si layer;

d) masking said nMOS site formed by step c), forming an a-Si layer over said pMOS site using a second heavy ion implantation with a material selected from the group consisting of Ge and Si, and implanting boron solely into said a –Si regions;

e) laser annealing said nMOS and pMOS sites with a pulse having a period of time of between about 40 ns and about 80 ns and at an energy level sufficient to melt at least a portion of the a- Si but insufficient to melt the polysilicon; and

f) affecting cooling after laser annealing to convert a- Si into polysilicon without gate oxide damage.

12. (Previously Presented) In a method of making a dual work function gate electrode of a CMOS semiconductor structure, the improvement comprising formation of the dual work function gate electrode so that there is no boron penetration in the channel region and no boron depletion near the gate oxide, comprising:

a) forming a gate oxide layer over a channel of a nMOS site and over a channel of a pMOS site;

b) forming an undoped polysilicon layer over said gate oxide layer;

c) masking said pMOS site, forming an a-Si layer over said nMOS site using a first heavy ion implantation, and implanting arsenic solely into said a- Si layer;

d) masking said nMOS site formed by step c), forming an a-Si layer over said pMOS site using a second heavy ion implantation, and implanting boron solely into said a –Si regions;

e) laser annealing said nMOS and pMOS sites with a pulse having a period of time of between about 40 ns and about 80 ns and at an energy level sufficient to melt at least a portion of the a- Si but insufficient to melt the polysilicon; and

f) affecting cooling after laser annealing to convert a- Si into polysilicon without gate oxide damage.

13. (Previously Presented) The method of claim 12 wherein said laser energy level sufficient to melt at least a portion of a- Si but insufficient to melt said polysilicon is between about 0.3 J/cm^2 to about 0.7 J/cm^2.

14. (Previously Presented) The method of claim 12 wherein in step d) said boron implanting in said a- Si regions is in a concentration range from about 1×10^{19} cm^{-3} to about 5×10^{20} cm^{-3}.

15. (Previously Presented) The method of claim 1 wherein said layer of undoped polysilicon has a thickness of between about 50Å and about 200Å